Atty Docket No.: M4065.0489/P489-A

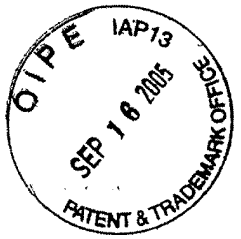
Inventor: Donald L. Yates et al.

Application No.: 10/734,201-Conf. #4789 **Filing Date:** December 15, 2003
Title: METHOD OF IMPROVING SURFACE PLANARITY PRIOR TO MRAM BIT MATERIAL DEPOSITION

Documents Filed:

Amendment Transmittal (1 page)

Amendment (13 pages)



Via: PTO Courier
Sender's Initials: TJD/PAV/kh **Date:** September 16, 2005

RAJ

Docket No.: M4065.0489/P489-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Donald L. Yates et al.

Application No.: 10/734,201 | Confirmation No.: 4789

Filed: December 15, 2003 | Art Unit: 2812

For: DEVICE HAVING IMPROVED SURFACE PLANARITY PRIOR TO MRAM BIT MATERIAL DEPOSITION (amended) | Examiner: H. J. Tsai

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated June 16, 2005 (Paper No. 0605), please amend the above-identified U.S. patent application as follows:

Amendments to the Specification are shown beginning on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 5 of this paper.

Remarks/Arguments begin on page 9 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please amend the Title of the Invention as follows:

DEVICE HAVING IMPROVED ~~METHOD OF IMPROVING~~ SURFACE PLANARITY PRIOR TO MRAM BIT MATERIAL DEPOSITION

Amend the specification as follows:

[0043] Hence, in an exemplary embodiment of the present invention as shown in FIG. 12, a second conductor layer or material layer 63 is formed over the upper surface of barrier layer 59, metal line 62 and insulating layer 54. Consequently, roughened portions 62a and protruding portions 59a are conformally covered by the second conductor layer 63. The second conductor layer 63 may comprise bonding materials such as tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) or chromium (Cr), among others. In a preferred embodiment of the invention, the conductor layer 63 is formed of sputtered tantalum. In this embodiment, tantalum is deposited to a thickness of about 5 nm to about 50 nm. In addition, this layer may be used as a series resistor by including a resistive material such as TaN, ~~WsiN~~ WSiN or other materials. The resistor layer can be deposited under the metal layer to be smoothed in order to preserve its thickness or in place of the conductor layer 63.

[0044] Next, as shown in FIG. 13, second conductor layer 63 is lightly polished to provide a planar surface for the subsequent fabrication of MRAM structures 100 (as described below). The term "lightly polished" is defined herein as polishing enough to planarize or flatten the second conductor layer 63 but not enough to pattern define. In other words, a top portion of the second conductor layer 63 is planarized and a lower portion of the second conductor layer 63 remains intact, conformally covering

roughened portions 62a and protruding portions 59a. The portions of conductor layer 63 overlying insulating layer 54 ~~is~~ are etched in subsequent steps (i.e., defining of the magnetic stack). Note, although roughened portions 62a and protruding portions 59a are not shown, they are still present in the intermediate structure of FIG. 13. However, as noted above, they are covered by the planarized second conductor layer 63 and ~~has~~ have been omitted from FIG. 13 for simplicity. Further, in the proceeding Figures, conductor layer 63 is shown as simply the interface for the MRAM structure 100 and the metal line 62/barrier layer 59.

[0050] In an exemplary embodiment of the present invention, the conductive layer 85 may be formed of tungsten nitrogen (WN), which is deposited to a thickness of about 100-400 Angstroms, more preferably of about 200-300 Angstroms. However, the invention is not limited to this exemplary embodiment[[,]]; this layer may be comprised of a resistive material such as WN, TaN, ~~WsiN~~ WSiN, and others. This layer may act as a series resistor and or a ~~cmp~~ CMP stopping layer dependent on the material and thickness chosen. Materials such as a-c amorphous carbon, various oxides and nitrides may be used as ~~cmp~~ CMP stops as well as series resistors.

[0053] Subsequent to the formation of the insulating layer 95 (FIG. 19), portions of the insulating layer 95 that are formed over the top surface of the MRAM structures 100 are removed by means of chemical mechanical polishing (CMP) or well-known RIE dry etching processes. In an exemplary embodiment of the invention, the insulating layer 95 is chemical mechanical polished so that an abrasive ~~abravise~~ polish removes the top surface of the insulating layer 95 above the MRAM structures 100, down to or near the planar surface of the top surface of the conductive layer 85, to form respective MRAM contacts 99 in a polished insulating layer 96, as illustrated in FIG. 20.

This way, the conductive layer 85, which was formed as part of the sense layer 92 of the MRAM structure 100, acts as a polishing stop layer in the formation of the contacts 99.

AMENDMENTS TO THE CLAIMS

1-21. (canceled)

22. (currently amended) A magnetic random access memory structure comprising:

an insulating layer;

a planarized barrier layer disposed over the insulating layer;

plurality of longitudinally extending planarized conductive lines formed over ~~an insulating~~ said barrier layer ~~of a semiconductor substrate~~;

respective first magnetic layers over said conductive lines;

respective second magnetic layers over said first magnetic layers; and

a planarized conductive material layer formed between said planarized conductive lines and said barrier layer, and said first magnetic layers.

23. (previously presented) The structure of claim 22 wherein said conductive material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

24. (previously presented) The structure of claim 22 wherein said conductive material layer is a resistive material.

25. (original) The structure of claim 22 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

26. (previously presented) The structure of claim 22 wherein said conductive material layer is formed to a thickness of about 5 nm to about 20 nm.

27. (original) The structure of claim 22 wherein said conductive lines are formed in a trench formed in said substrate.

28. (currently amended) A memory device comprising:

at least one magnetic random access memory cell, said magnetic random access memory cell comprising:

an insulating layer;

a planarized barrier layer formed over the insulating layer;

a planarized conductor formed over the planarized barrier layer;

a first ferromagnetic layer formed over said ~~a first~~ planarized conductor[[,]];

a second ferromagnetic layer formed over said first ferromagnetic layer[[,]];

a nonmagnetic layer between said first and second ferromagnetic layers[[,]]; and

a planarized conductive material layer provided between said ~~first~~ planarized conductor and said planarized barrier layer, and said first ferromagnetic layer.

29. (previously presented) The device of claim 28 wherein said conductive material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

30. (previously presented) The device of claim 28 wherein said conductive material layer is a resistive material.

31. (original) The device of claim 28 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 or polyimide.

32. (previously presented) The device of claim 28 wherein said conductive material layer is formed to a thickness of about 5 nm to about 20 nm.

33. (previously presented) The device of claim 28 wherein said planarized ~~first~~ conductor is formed in a trench of a substrate.

34-39. (canceled)

40. (new) The structure of claim 22, wherein respective first magnetic layers over said conductive lines are also over said planarized barrier layer.

41. (new) The device of claim 28, wherein the first ferromagnetic layer formed over said planarized conductor also is formed over said planarized barrier layer.

REMARKS

Claims 22-33 were pending. Claims 22 and 28 have been amended for clarity. Claims 40 and 41 are new. Claims 22-33 and 40-41 are pending.

Claims 22-33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,709,874 to Ning. Applicant respectfully requests reconsideration of this rejection.

Claim 22 recites an MRAM structure that includes "an insulating layer," "a planarized barrier layer disposed over the insulating layer," a "plurality of longitudinally extending planarized conductive lines formed over said barrier layer," "respective first magnetic layers over said conductive lines," "respective second magnetic layers over said first magnetic layers," and "a planarized conductive material layer formed between said planarized conductive lines and said barrier layer, and said first magnetic layers."

Ning discloses an MRAM structure in which upper portions of conductive material formed in barrier-lined trenches is removed to form recesses. A metal cap layer is formed in the recesses. The metal cap is not formed "over" the "barrier layer" as in recited claim 22. Ning does not anticipate claim 22.

Claim 22 is patentable over Ning. Claims 23-27 depend directly from claim 22 and are patentable over Ning for at least the same reasons.

Claim 28 recites a memory device that includes "at least one magnetic random access memory cell." The magnetic random access memory cell includes "an insulating layer," "a planarized barrier layer formed over the insulating layer," "a planarized conductor formed over the planarized barrier layer," "a first ferromagnetic layer formed over said planarized conductor," "a second ferromagnetic layer formed

over said first ferromagnetic layer," "a nonmagnetic layer between said first and second ferromagnetic layers," and "a planarized conductive material layer provided between said planarized conductor and said planarized barrier layer, and said first ferromagnetic layer."

Ning discloses that a memory device in which a conductive metal cap is formed in a recess formed in a conductive layer. Ning does not teach a memory device with at least one magnetic random access memory cell that has "a planarized barrier layer formed over [an] insulating layer," a "planarized conductor formed over the planarized barrier layer," and "a planarized conductive material layer provided between said planarized conductor and said planarized barrier layer."

Claim 28 is patentable over Ning. Claims 29-33 depend directly from claim 28 and are patentable over Ning for at least the same reasons.

Claims 22, 25, 27-28, 31, and 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,555,858 to Jones et al. Applicant respectfully requests reconsideration of this rejection.

Claim 22 recites an MRAM structure that includes "a planarized barrier layer" disposed over an insulating layer, a "plurality of longitudinally extending planarized conductive lines formed over said barrier layer," and "a planarized conductive material layer formed between said planarized conductive lines and said barrier layer," and first magnetic layers "formed over said conductive lines."

Jones et al. discloses an MRAM structure in which a dielectric layer 230 is formed over barrier layers 226. Conductive layer 232 is formed over the dielectric layer 230. Jones et al. does not disclose an MRAM structure with "a planarized conductive

material layer formed between...planarized conductive lines and [a] barrier layer," and first magnetic layers "formed over said conductive lines."

Claim 22 is patentable over Jones et al. Claims 25 and 27 depend directly from claim 22 and are patentable over Jones et al. for at least the same reasons.

Claim 28 recites a memory device that includes an MRAM cell having a "planarized barrier layer" formed over an insulating layer and "a planarized conductor formed over the planarized barrier layer." A planarized conductive material layer is "provided between said planarized conductor and said planarized barrier layer," and a first ferromagnetic layer "formed over said planarized conductor."

Jones et al. discloses a memory device featuring dielectric layer 230 formed over barrier layers 236. Jones et al. does not disclose a memory device with an MRAM cell that has "a planarized conductive material layer provided between said planarized conductor and said planarized barrier layer," and a first ferromagnetic layer "formed over said planarized conductor."

Claim 28 is patentable over Jones et al. Claims 31 and 33 depend from claim 28 and are patentable over Jones et al. for at least the same reasons.

Claims 22-33 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting over claims 43-67 of copending U.S. Pat. Appl. No. 10/196,933. Applicant will address the rejection when it is no longer provisional.

Claims 23-24, 26, 29-30, and 32 stand rejected under 35 U.S.C. § 103 as being unpatentable over Jones et al. in view of Ning. Applicant respectfully requests reconsideration of this rejection.

Claims 23, 24, and 26 depend directly from claim 22. Claim 22 is patentable over Jones et al. as advanced above. Claim 22 also is patentable over Ning. Ning does not remedy the deficiencies of Jones et al. Ning has been cited as providing thickness ranges and materials missing from Jones. Even if Jones et al. and Ning were combined, the result would be an MRAM structure in which a portion of conductor 228 is removed to provide a recess for conductive layer 232. Ning does not combine with Jones to provide an MRAM structure with "a planarized conductive material layer formed between...planarized conductive lines and [a] barrier layer," and first magnetic layers "formed over said conductive lines."

Claim 22 is patentable over Jones et al. in view of Ning. Claims 23, 24, and 26 depend from claim 22 and are patentable over Jones et al. in view of Ning for at least the same reasons.

Claims 29, 30, and 32 depend directly from claim 28. Claim 28 is patentable over Jones et al. as advanced above. Claims 28 also is patentable over Ning. Ning does not remedy the deficiencies of Jones et al. Ning has been cited to provide thickness ranges and materials missing from Jones et al. Even if Jones et al. and Ning were combined, the result would be a memory device in which a portion of conductor 228 is removed to provide a recess for conductive layer 232. Ning does not combine with Jones et al. to provide a memory device with a planarized conductive material layer is "provided between said planarized conductor and said planarized barrier layer," and a first ferromagnetic layer "formed over said planarized conductor."

Claim 28 is patentable over Jones et al. in view of Ning. Claims 29, 30, and 32 are patentable over Jones et al. in view of Ning for at least the same reasons.

New claims 40 and 41 depend from claims 22 and 28 respectively, which are patentable over the cited prior art as advanced above. Claims 40 and 41 are patentable over the cited prior art for at least the same reasons.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: September 16, 2005

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicant